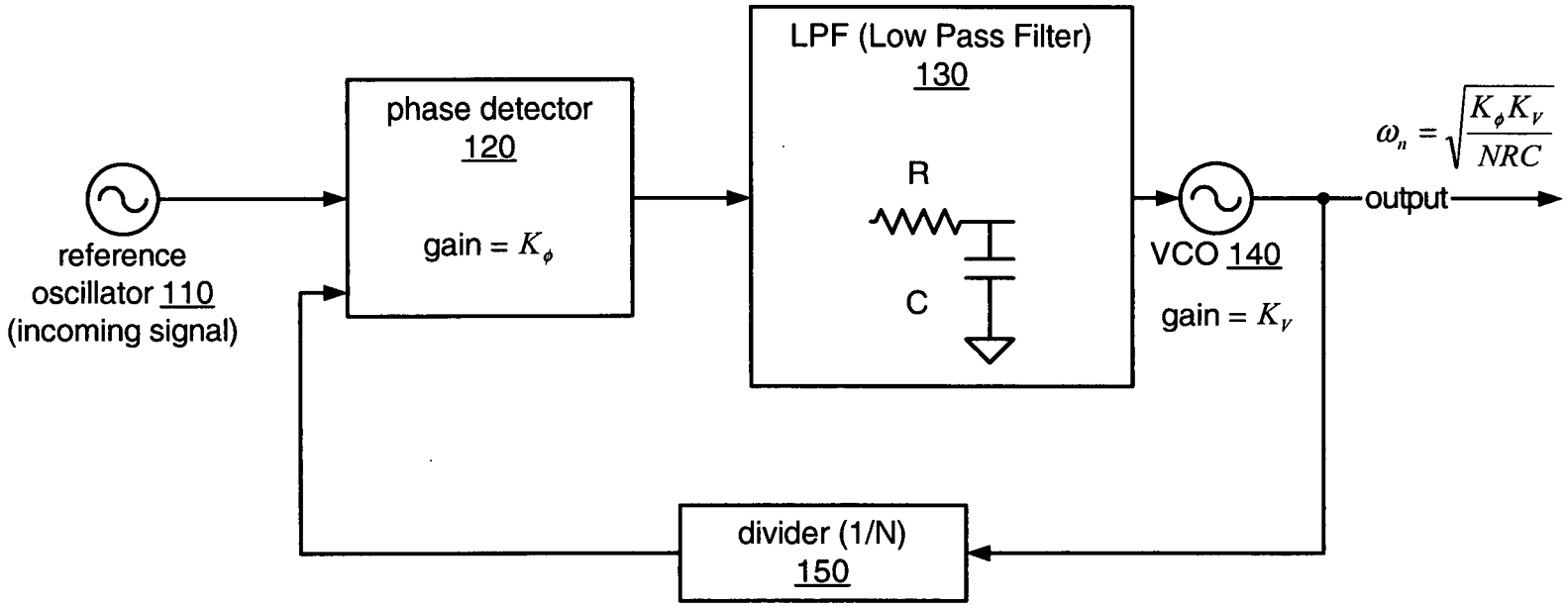
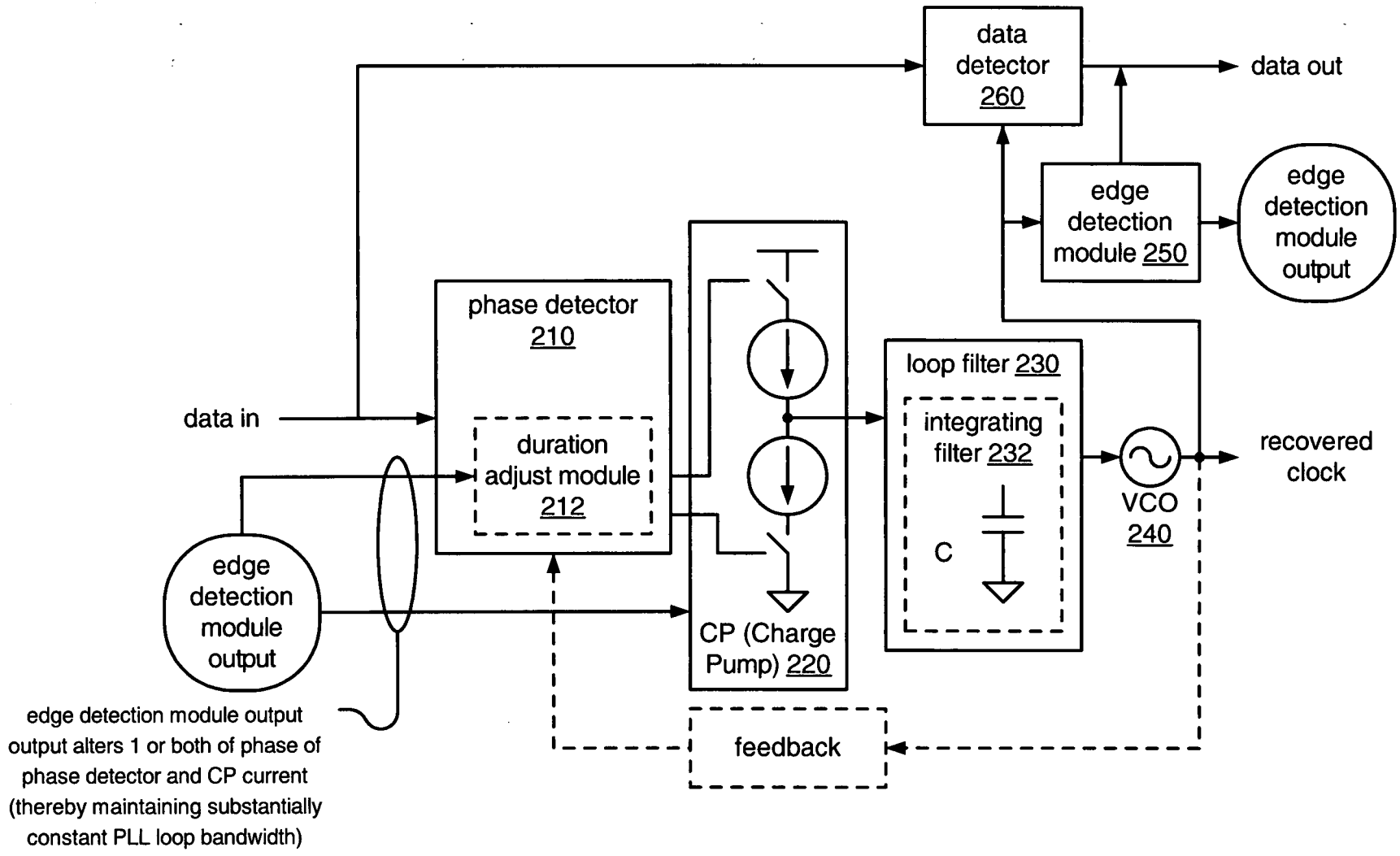


PLL (Phase Locked Loop)

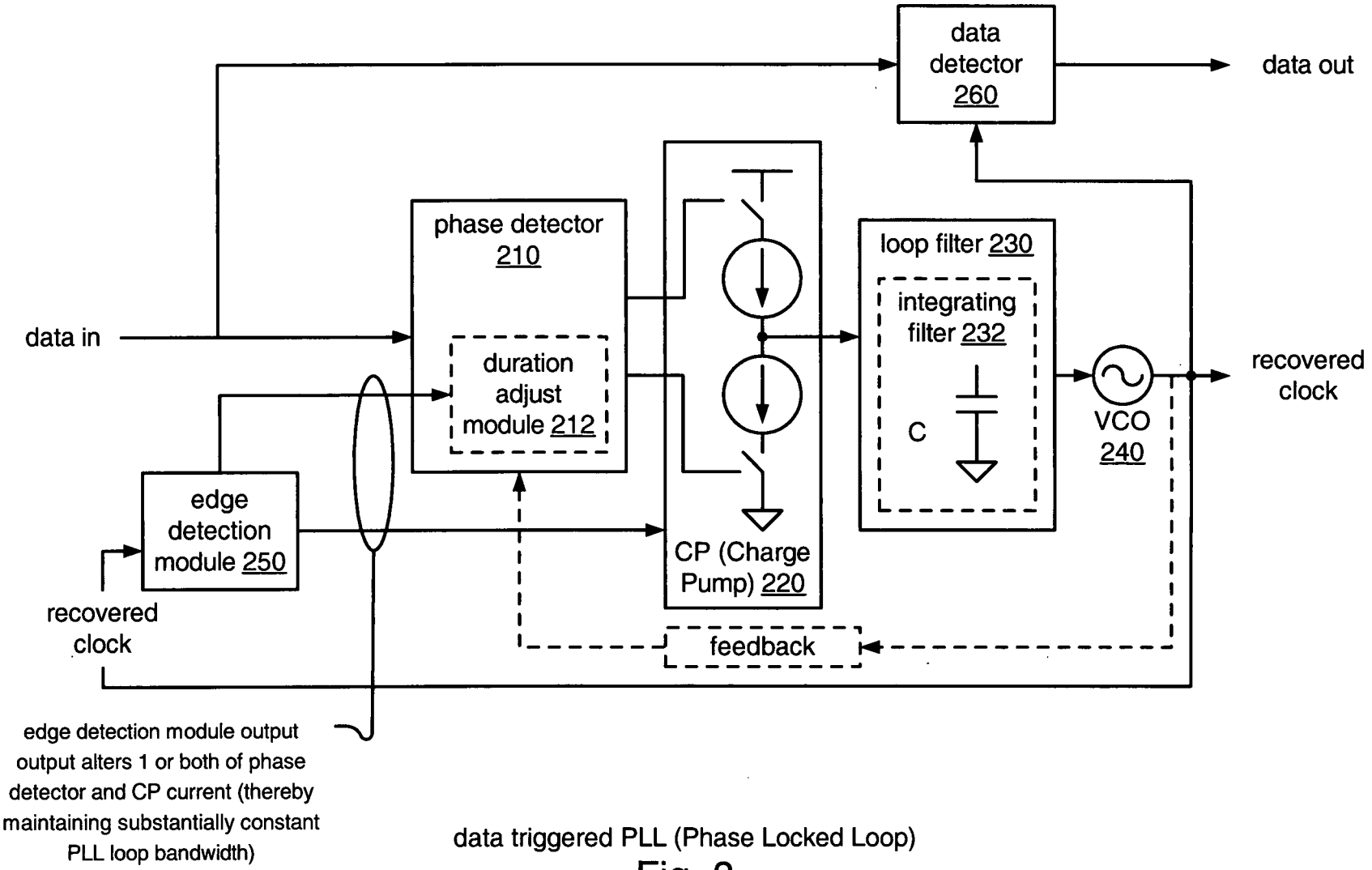
Fig. 1

(prior art)



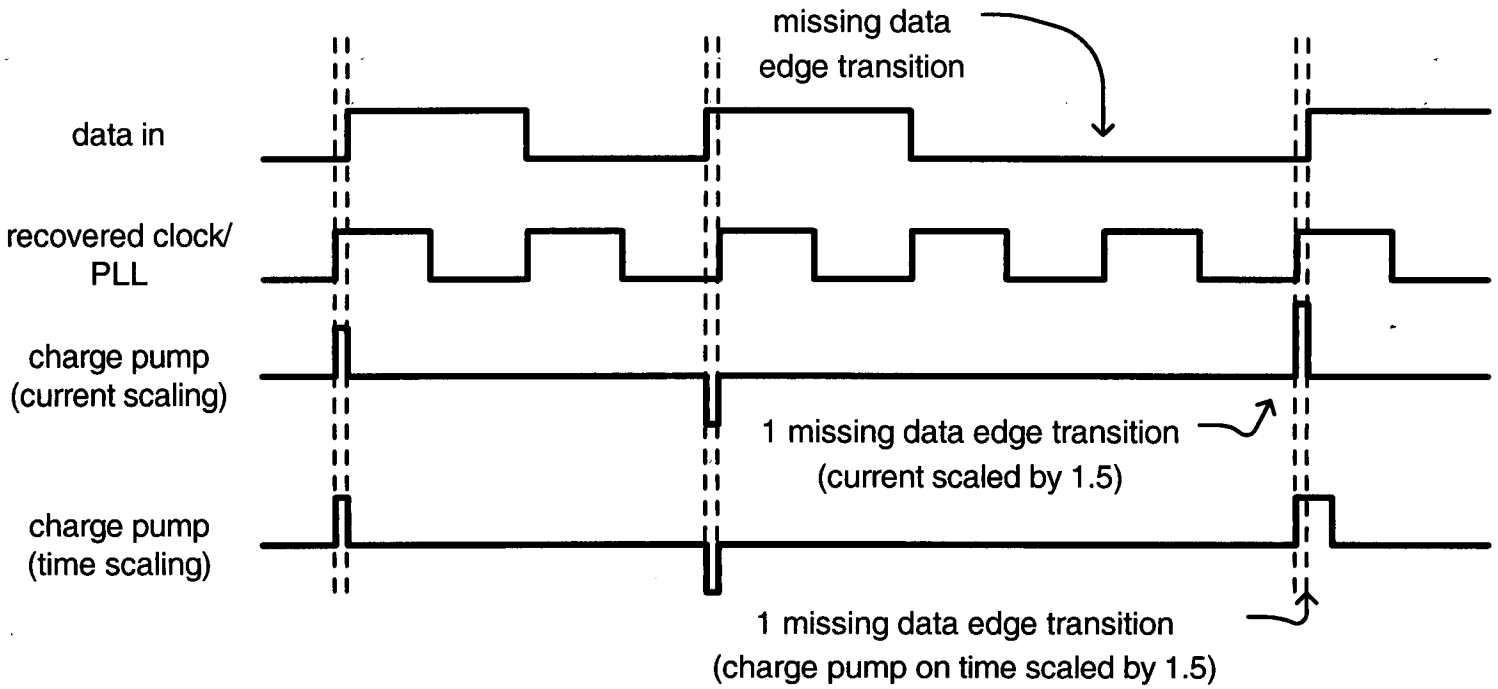
data triggered PLL (Phase Locked Loop)

Fig. 2



data triggered PLL (Phase Locked Loop)

Fig. 3

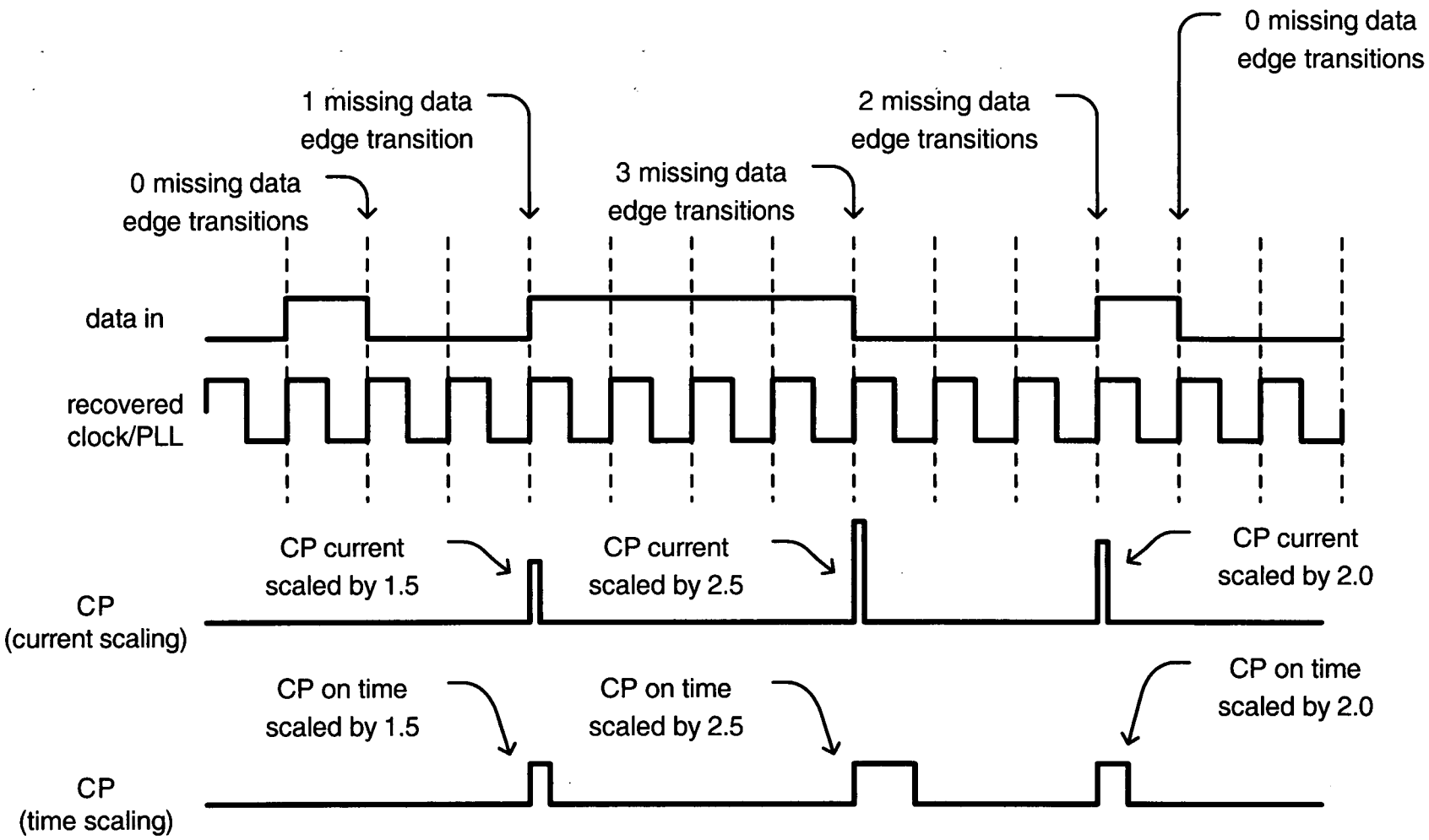


# missing data edge transitions	phase error normalized to 1 on edges					sum
0					1	1
1				1/2	2/2	1.5
2			1/3	2/3	3/3	2.0
3		1/4	2/4	3/4	4/4	2.5
4	1/5	2/5	3/5	4/5	5/5	3.0
...					...	...

may alternatively implement non-linear shift in PLL phase relative to data phase in absence of data edge transitions

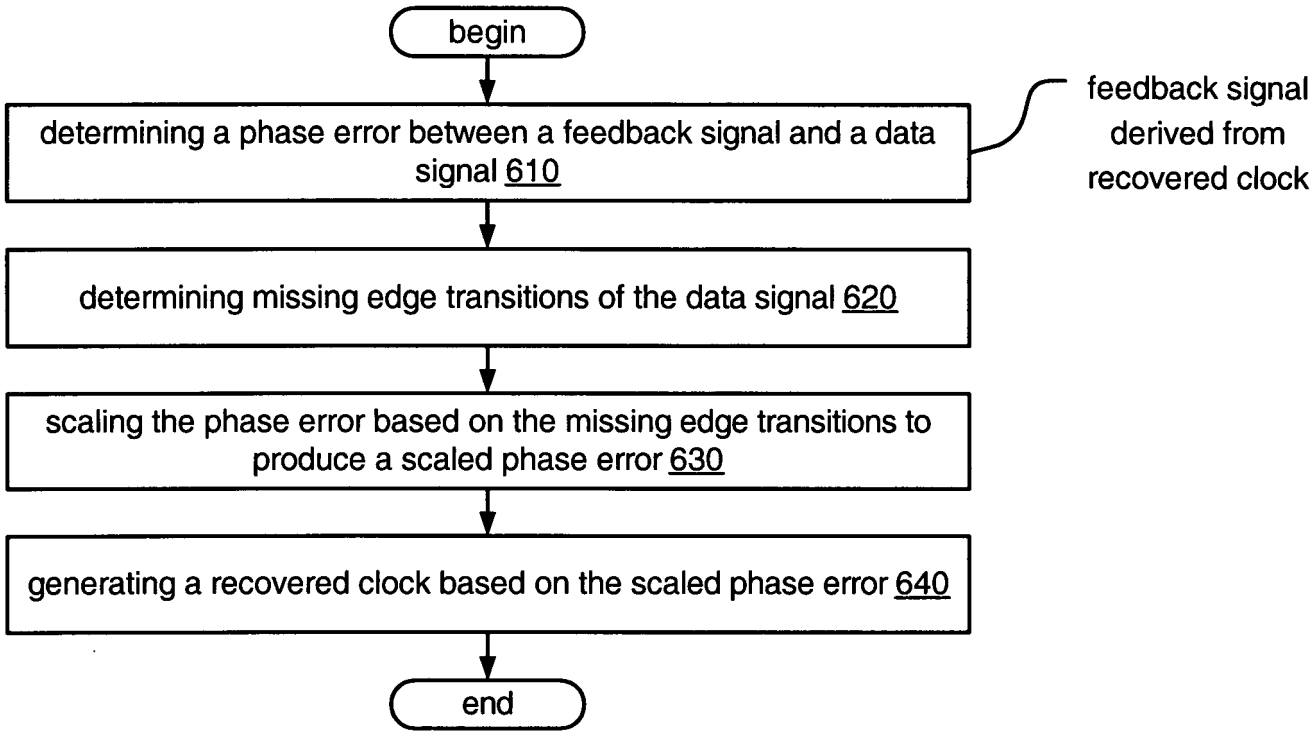
programmable CP current (or on time) that adapts to data edge transition density within data triggered PLL

Fig. 4



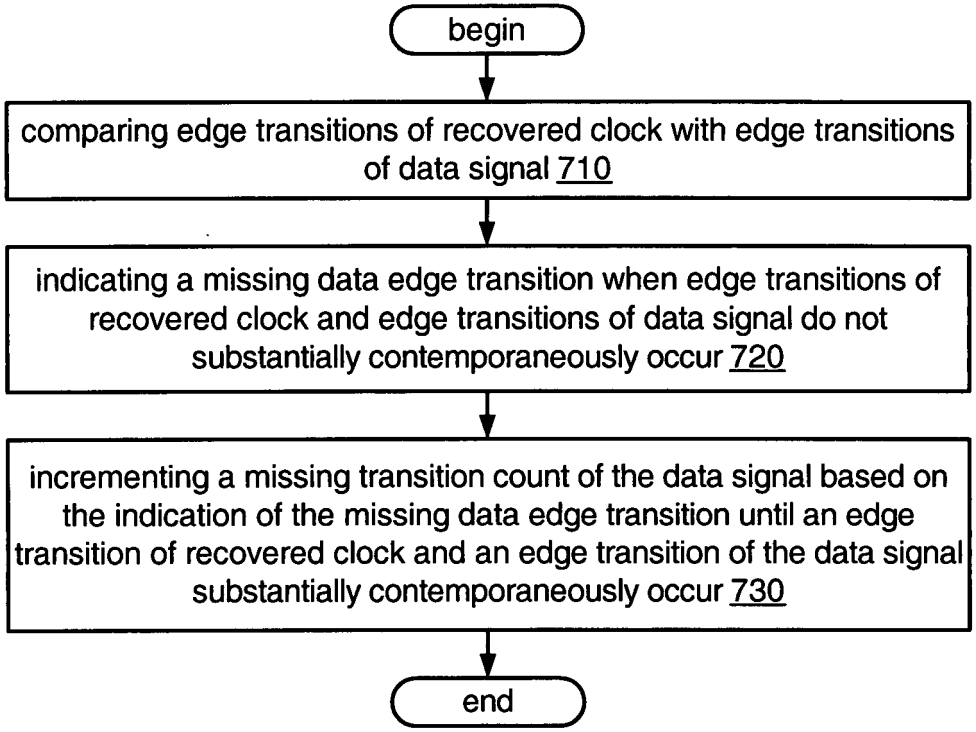
programmable CP current (or on time) that adapts to data edge transition density within data triggered PLL

Fig. 5



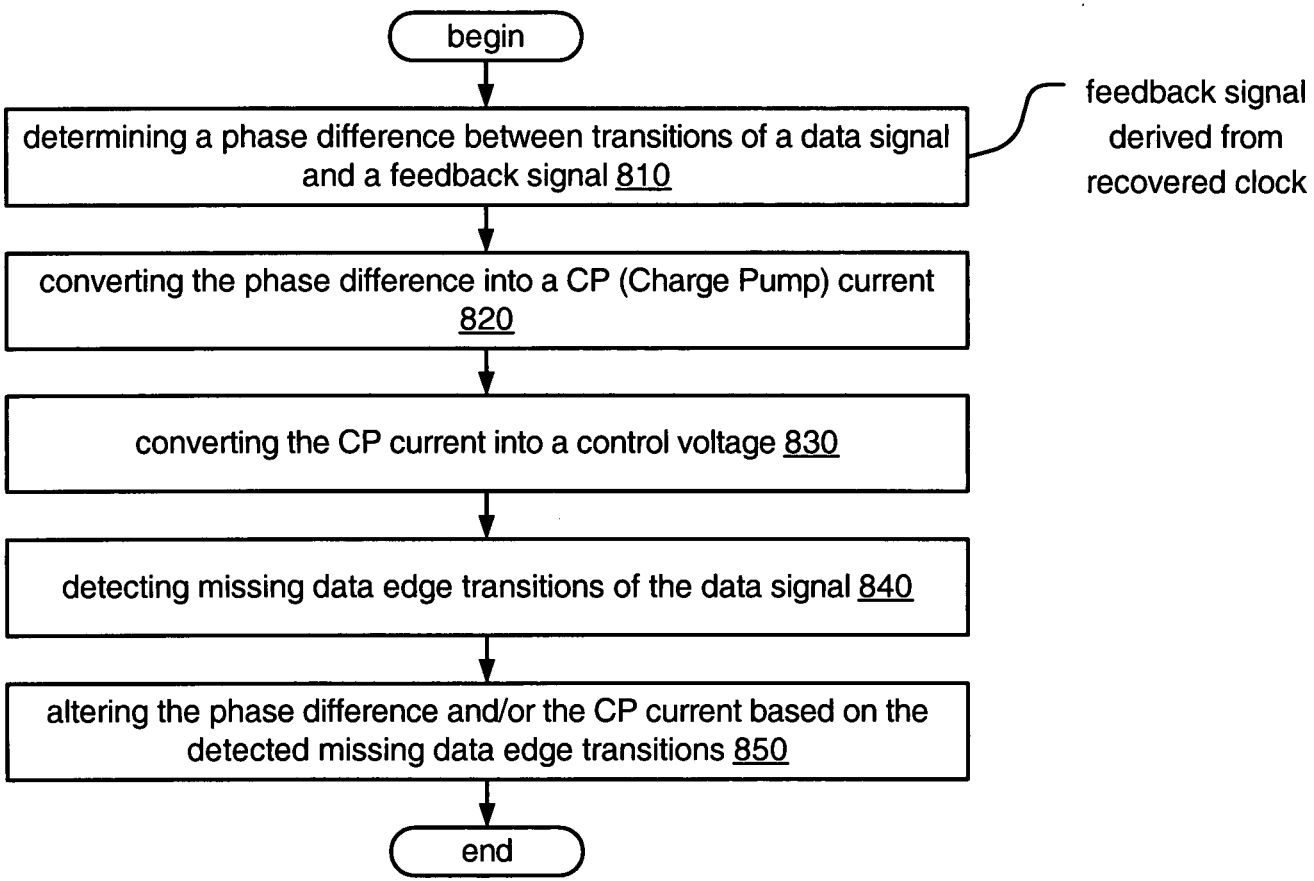
method for recovering clock from a data signal

Fig. 6



method for determining missing edge transitions of the data signal

Fig. 7



method for recovering clock from a data signal

Fig. 8